

EXPERIMENT NO: 10

AIM: TO DESIGN & VERIFY OPERATION OF HALF ADDER & FULL ADDER.

APPARATUS REQUIRED: Power supply, IC's , Digital Trainer, Connecting leads .

BRIEF THEORY: We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

Half Adder: It is a logic circuit that adds two bits. It produces the O/P, sum & carry. The Boolean equation for sum & carry are

$$\text{SUM} = A + B$$

$$\text{CARRY} = A \cdot B$$

Therefore, sum produces 1 when A&B are different and carry is 1 when A&B are 1. Application of Half adder is limited.

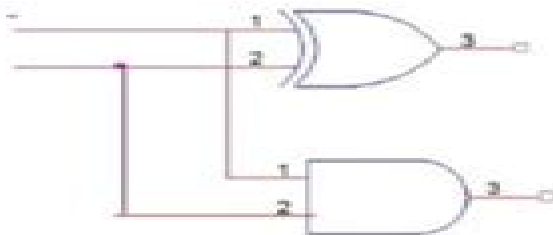
Full Adder: It is a logic circuit that can add three bits. It produces two O/P sum & carry. The Boolean Equation for sum & carry are

$$\text{SUM} = A + B + C$$

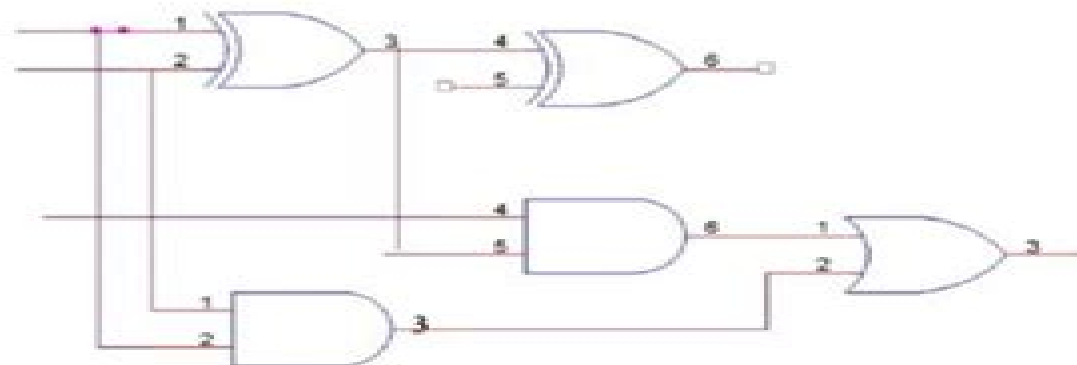
$$\text{CARRY} = A \cdot B + (A + B) \cdot C$$

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

CIRCUIT DAIGRAM



HALF ADDER



FULL ADDER

Physics Lab Manual Half Adder

Kathleen Armour



Physics Lab Manual Half Adder:

Computers; Selected Bibliographic Citations Announced in U.S. Government Research and Development Reports, 1966 United States. Office of State Technical Services,1968 **U.S. Government Research & Development Reports ,1967-10** *Instrumentation Technology ,1968* **Government Reports Announcements & Index ,1993**
Bibliography of Scientific and Industrial Reports ,1967 **Government Reports Announcements ,1967** **Nuclear Science Abstracts ,1965** *Books in Print Supplement ,1979* *InfoWorld ,1983-06-13* InfoWorld is targeted to Senior IT professionals Content is segmented into Channels and Topic Centers InfoWorld also celebrates people companies and projects *Proceedings of the IRE. Institute of Radio Engineers,1957*

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