

Mario Nemirowsky · Dean M. Tullsen

Multithreading Architecture

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**Brandon Reagen, Robert Adolf, Paul
Whatmough, Gu-Yeon Wei, David
Brooks**



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Multithreading Architecture Mario Nemirovsky, Dean M. Tullsen, 2013 Multithreaded architectures now appear across the entire range of computing devices from the highest performing general purpose devices to low end embedded processors Multithreading enables a processor core to more effectively utilize its computational resources as a stall in one thread need not cause execution resources to be idle This enables the computer architect to maximize performance within area constraints power constraints or energy constraints However the architectural options for the processor designer or architect looking to implement multithreading are quite extensive and varied as evidenced not only by the research literature but also by the variety of commercial implementations This book introduces the basic concepts of multithreading describes a number of models of multithreading and then develops the three classic models coarse grain fine grain and simultaneous multithreading in greater detail It describes a wide variety of architectural and software design tradeoffs as well as opportunities specific to multithreading architectures Finally it details a number of important commercial and academic hardware implementations of multithreading

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Architectural and Operating System Support for Virtual Memory Abhishek Bhattacharjee, Daniel Lustig, 2022-05-31
This book provides computer engineers, academic researchers, new graduate students, and seasoned practitioners an end-to-end overview of virtual memory. We begin with a recap of foundational concepts and discuss not only the state of the art in virtual memory hardware and software support available today, but also emerging research trends in this space. The span of topics covers processor microarchitecture, memory systems, operating system design, and memory allocation. We show how efficient virtual memory implementations hinge on careful hardware and software cooperation, and we discuss new research directions aimed at addressing emerging problems in this space. Virtual memory is a classic computer science abstraction and one of the pillars of the computing revolution. It has long enabled hardware flexibility, software portability, and overall better security, to name just a few of its powerful benefits. Nearly all user-level programs today take for granted that they will have been freed from the burden of physical memory management by the hardware, the operating system, device drivers, and system libraries. However, despite its ubiquity in systems ranging from warehouse-scale datacenters to embedded Internet of Things (IoT) devices, the overheads of virtual memory are becoming a critical performance bottleneck today. Virtual memory architectures designed for individual CPUs or even individual cores are, in many cases, struggling to scale up and scale out to today's systems, which now increasingly include exotic hardware accelerators such as GPUs, FPGAs, or DSPs, and emerging memory technologies such as non-volatile memory, and which run increasingly intensive workloads such as virtualized and/or big data applications. As such, many of the fundamental abstractions and implementation approaches for virtual memory are being augmented, extended, or entirely rebuilt in order to ensure that virtual memory remains viable and performant in the years to come.

Security Basics for Computer Architects Ruby B. Lee, 2022-05-31
Design for security is an essential aspect of the design of future computers. However, security is not well understood by the computer architecture community. Many important security aspects have evolved over the last several decades in the cryptography, operating systems, and networking communities. This book attempts to introduce the computer architecture student, researcher, or practitioner to the basic concepts of security and threat-based design. Past work in different security communities can inform our thinking and provide a rich set of technologies for building

architectural support for security into all future computers and embedded computing devices and appliances I have tried to keep the book short which means that many interesting topics and applications could not be included What the book focuses on are the fundamental security concepts across different security communities that should be understood by any computer architect trying to design or evaluate security aware computer architectures

Datacenter Design and Management

Benjamin C. Lee,2022-05-31 An era of big data demands datacenters which house the computing infrastructure that translates raw data into valuable information This book defines datacenters broadly as large distributed systems that perform parallel computation for diverse users These systems exist in multiple forms private and public and are built at multiple scales Datacenter design and management is multifaceted requiring the simultaneous pursuit of multiple objectives Performance efficiency and fairness are first order design and management objectives which can each be viewed from several perspectives This book surveys datacenter research from a computer architect s perspective addressing challenges in applications design management server simulation and system simulation This perspective complements the rich bodies of work in datacenters as a warehouse scale system which study the implications for infrastructure that encloses computing equipment and in datacenters as distributed systems which employ abstract details in processor and memory subsystems This book is written for first or second year graduate students in computer architecture and may be helpful for those in computer systems The goal of this book is to prepare computer architects for datacenter oriented research by describing prevalent perspectives and the state of the art

Deep Learning for Computer Architects

Brandon Reagen,Robert Adolf,Paul Whatmough,Gu-Yeon Wei,David Brooks,2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various

contributions fall in context Single-Instruction Multiple-Data Execution Christopher J. Hughes, 2022-05-31 Having hit power limitations to even more aggressive out of order execution in processor cores many architects in the past decade have turned to single instruction multiple data SIMD execution to increase single threaded performance SIMD execution or having a single instruction drive execution of an identical operation on multiple data items was already well established as a technique to efficiently exploit data parallelism Furthermore support for it was already included in many commodity processors However in the past decade SIMD execution has seen a dramatic increase in the set of applications using it which has motivated big improvements in hardware support in mainstream microprocessors The easiest way to provide a big performance boost to SIMD hardware is to make it wider i e increase the number of data items hardware operates on simultaneously Indeed microprocessor vendors have done this However as we exploit more data parallelism in applications certain challenges can negatively impact performance In particular conditional execution non contiguous memory accesses and the presence of some dependences across data items are key roadblocks to achieving peak performance with SIMD execution This book first describes data parallelism and why it is so common in popular applications We then describe SIMD execution and explain where its performance and energy benefits come from compared to other techniques to exploit parallelism Finally we describe SIMD hardware support in current commodity microprocessors This includes both expected design tradeoffs as well as unexpected ones as we work to overcome challenges encountered when trying to map real software to SIMD execution *On-Chip Photonic Interconnects* Christopher J. Nitta, Matthew Farrens, Venkatesh Akella, 2022-06-01 As the number of cores on a chip continues to climb architects will need to address both bandwidth and power consumption issues related to the interconnection network Electrical interconnects are not likely to scale well to a large number of processors for energy efficiency reasons and the problem is compounded by the fact that there is a fixed total power budget for a die dictated by the amount of heat that can be dissipated without special and expensive cooling and packaging techniques Thus there is a need to seek alternatives to electrical signaling for on chip interconnection applications Photonics which has a fundamentally different mechanism of signal propagation offers the potential to not only overcome the drawbacks of electrical signaling but also enable the architect to build energy efficient scalable systems The purpose of this book is to introduce computer architects to the possibilities and challenges of working with photons and designing on chip photonic interconnection networks **General-Purpose Graphics Processor Architectures** Tor M. Aamodt, Wilson Wai Lun Fung, Timothy G. Rogers, 2022-05-31 Originally developed to support video games graphics processor units GPUs are now increasingly used for general purpose non graphics applications ranging from machine learning to mining of cryptographic currencies GPUs can achieve improved performance and efficiency versus central processing units CPUs by dedicating a larger fraction of hardware resources to computation In addition their general purpose programmability makes contemporary GPUs appealing to software developers in comparison to domain specific accelerators This book provides an

introduction to those interested in studying the architecture of GPUs that support general purpose computing It collects together information currently only found among a wide range of disparate sources The authors led development of the GPGPU Sim simulator widely used in academic research on GPU architectures The first chapter of this book describes the basic hardware structure of GPUs and provides a brief overview of their history Chapter 2 provides a summary of GPU programming models relevant to the rest of the book Chapter 3 explores the architecture of GPU compute cores Chapter 4 explores the architecture of the GPU memory system After describing the architecture of existing systems Chapters 3 and 4 provide an overview of related research Chapter 5 summarizes cross cutting research impacting both the compute core and memory system This book should provide a valuable resource for those wishing to understand the architecture of graphics processor units GPUs used for acceleration of general purpose applications and to those who want to obtain an introduction to the rapidly growing body of research exploring how to improve the architecture of these GPUs

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