

PERFORMANCE MODELING FOR COMPUTER ARCHITECTS

C. M. Krishna



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Performance Modeling For Computer Architects Systems

C. M. Krishna



Performance Modeling For Computer Architects Systems:

Performance Modeling for Computer Architects C. M. Krishna, 1995-10-14 As computers become more complex the number and complexity of the tasks facing the computer architect have increased Computer performance often depends in complex way on the design parameters and intuition that must be supplemented by performance studies to enhance design productivity This book introduces computer architects to computer system performance models and shows how they are relatively simple inexpensive to implement and sufficiently accurate for most purposes It discusses the development of performance models based on queuing theory and probability The text also shows how they are used to provide quick approximate calculations to indicate basic performance tradeoffs and narrow the range of parameters to consider when determining system configurations It illustrates how performance models can demonstrate how a memory system is to be configured what the cache structure should be and what incremental changes in cache size can have on the miss rate A particularly deep knowledge of probability theory or any other mathematical field to understand the papers in this volume is not required

Computer Architecture Performance Evaluation Methods Lieven Eeckhout, 2022-05-31 Performance evaluation is at the foundation of computer architecture research and development Contemporary microprocessors are so complex that architects cannot design systems based on intuition and simple models only Adequate performance evaluation methods are absolutely crucial to steer the research and development process in the right direction However rigorous performance evaluation is non trivial as there are multiple aspects to performance evaluation such as picking workloads selecting an appropriate modeling or simulation approach running the model and interpreting the results using meaningful metrics Each of these aspects is equally important and a performance evaluation method that lacks rigor in any of these crucial aspects may lead to inaccurate performance data and may drive research and development in a wrong direction The goal of this book is to present an overview of the current state of the art in computer architecture performance evaluation with a special emphasis on methods for exploring processor architectures The book focuses on fundamental concepts and ideas for obtaining accurate performance data The book covers various topics in performance evaluation ranging from performance metrics to workload selection to various modeling approaches including mechanistic and empirical modeling And because simulation is by far the most prevalent modeling technique more than half the book's content is devoted to simulation The book provides an overview of the simulation techniques in the computer designer's toolbox followed by various simulation acceleration techniques including sampled simulation statistical simulation parallel simulation and hardware accelerated simulation Table of Contents Introduction Performance Metrics Workload Design Analytical Performance Modeling Simulation Sampled Simulation Statistical Simulation Parallel Simulation and Hardware Acceleration Concluding Remarks

Computer Architecture Michael J. Flynn, 1995 Computer Architecture Software Engineering
NBS Special Publication ,1968 Modeling and Optimization of Parallel and Distributed Embedded Systems Arslan

Munir,Ann Gordon-Ross,Sanjay Ranka,2016-02-08 This book introduces the state of the art in research in parallel and distributed embedded systems which have been enabled by developments in silicon technology micro electro mechanical systems MEMS wireless communications computer networking and digital electronics These systems have diverse applications in domains including military and defense medical automotive and unmanned autonomous vehicles The emphasis of the book is on the modeling and optimization of emerging parallel and distributed embedded systems in relation to the three key design metrics of performance power and dependability Key features Includes an embedded wireless sensor networks case study to help illustrate the modeling and optimization of distributed embedded systems Provides an analysis of multi core many core based embedded systems to explain the modeling and optimization of parallel embedded systems Features an application metrics estimation model Markov modeling for fault tolerance and analysis and queueing theoretic modeling for performance evaluation Discusses optimization approaches for distributed wireless sensor networks high performance and energy efficient techniques at the architecture middleware and software levels for parallel multicore based embedded systems and dynamic optimization methodologies Highlights research challenges and future research directions The book is primarily aimed at researchers in embedded systems however it will also serve as an invaluable reference to senior undergraduate and graduate students with an interest in embedded systems research System-on-Chip

Methodologies & Design Languages Peter J. Ashenden,Jean Mermet,Ralf Seepold,2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field **Scientific and Technical Aerospace Reports** ,1994 **Electronic**

Design Automation for IC System Design, Verification, and Testing Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on

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