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Grigorios Magklis

Processor Microarchitecture

An Implementation Perspective

Processor Microarchitecture An Implementation Perspective Fernando Latorre

**Antonio Gonzalez, Fernando
Latorre, Grigorios Magklis**



Processor Microarchitecture An Implementation Perspective Fernando Latorre:

Processor Microarchitecture Antonio Gonzalez, Fernando Latorre, Grigorios Magklis, 2022-05-31 This lecture presents a study of the microarchitecture of contemporary microprocessors. The focus is on implementation aspects with discussions on their implications in terms of performance, power, and cost of state-of-the-art designs. The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories. Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction. The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions. The next chapter presents the allocation stage and pays special attention to the implementation of register renaming. Afterward, the issue stage is studied. Here the logic to implement out-of-order issue for both memory and non-memory instructions is thoroughly described. The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance. Finally, the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations. This lecture is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture. It is also intended for practitioners in the industry in the area of microprocessor design. The book assumes that the reader is familiar with the main concepts regarding pipelining, out-of-order execution, cache memories, and virtual memory.

Table of Contents: Introduction, Caches, The Instruction Fetch Unit, Decode, Allocation, The Issue Stage, Execute, The Commit Stage, References, Author Biographies.

Single-Instruction Multiple-Data Execution Christopher J. Hughes, 2022-05-31 Having hit power limitations to even more aggressive out-of-order execution in processor cores, many architects in the past decade have turned to single instruction multiple data (SIMD) execution to increase single threaded performance. SIMD execution or having a single instruction drive execution of an identical operation on multiple data items was already well established as a technique to efficiently exploit data parallelism. Furthermore, support for it was already included in many commodity processors. However, in the past decade, SIMD execution has seen a dramatic increase in the set of applications using it, which has motivated big improvements in hardware support in mainstream microprocessors. The easiest way to provide a big performance boost to SIMD hardware is to make it wider, i.e., increase the number of data items hardware operates on simultaneously. Indeed, microprocessor vendors have done this. However, as we exploit more data parallelism in applications, certain challenges can negatively impact performance. In particular, conditional execution, non-contiguous memory accesses, and the presence of some dependences across data items are key roadblocks to achieving peak performance with SIMD execution. This book first describes data parallelism and why it is so common in popular applications. We then describe SIMD execution and explain where its performance and energy benefits come from compared to other

techniques to exploit parallelism Finally we describe SIMD hardware support in current commodity microprocessors This includes both expected design tradeoffs as well as unexpected ones as we work to overcome challenges encountered when trying to map real software to SIMD execution

On-Chip Photonic Interconnects Christopher J. Nitta,Matthew Farrens,Venkatesh Akella,2022-06-01 As the number of cores on a chip continues to climb architects will need to address both bandwidth and power consumption issues related to the interconnection network Electrical interconnects are not likely to scale well to a large number of processors for energy efficiency reasons and the problem is compounded by the fact that there is a fixed total power budget for a die dictated by the amount of heat that can be dissipated without special and expensive cooling and packaging techniques Thus there is a need to seek alternatives to electrical signaling for on chip interconnection applications Photonics which has a fundamentally different mechanism of signal propagation offers the potential to not only overcome the drawbacks of electrical signaling but also enable the architect to build energy efficient scalable systems The purpose of this book is to introduce computer architects to the possibilities and challenges of working with photons and designing on chip photonic interconnection networks

Principles of Secure Processor Architecture Design Jakub Szefer,2022-06-01 With growing interest in computer security and the protection of the code and data which execute on commodity computers the amount of hardware security features in today s processors has increased significantly over the recent years No longer of just academic interest security features inside processors have been embraced by industry as well with a number of commercial secure processor architectures available today This book aims to give readers insights into the principles behind the design of academic and commercial secure processor architectures Secure processor architecture research is concerned with exploring and designing hardware features inside computer processors features which can help protect confidentiality and integrity of the code and data executing on the processor Unlike traditional processor architecture research that focuses on performance efficiency and energy as the first order design objectives secure processor architecture design has security as the first order design objective while still keeping the others as important design aspects that need to be considered This book aims to present the different challenges of secure processor architecture design to graduate students interested in research on architecture and hardware security and computer architects working in industry interested in adding security features to their designs It aims to educate readers about how the different challenges have been solved in the past and what are the best practices i e the principles for design of new secure processor architectures Based on the careful review of past work by many computer architects and security researchers readers also will come to know the five basic principles needed for secure processor architecture design The book also presents existing research challenges and potential new research directions Finally this book presents numerous design suggestions as well as discusses pitfalls and fallacies that designers should avoid

AI for Computer Architecture Lizhong Chen,Drew Penney,Daniel Jiménez,2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact

on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs

Optimization and Mathematical Modeling in Computer Architecture Karthikeyan Sankaralingam, Michael Ferris, Tony Nowatzki, Cristian Estan, Nilay Vaish, David Wood, 2022-05-31 In this book we give an overview of modeling techniques used to describe computer systems to mathematical optimization tools We give a brief introduction to various classes of mathematical optimization frameworks with special focus on mixed integer linear programming which provides a good balance between solver time and expressiveness We present four detailed case studies instruction set customization data center resource management spatial architecture scheduling and resource allocation in tiled architectures showing how MILP can be used and quantifying by how much it outperforms traditional design exploration techniques This book should help a skilled systems designer to learn techniques for using MILP in their problems and the skilled optimization expert to understand the types of computer systems problems that MILP can be applied to

Quantum Computing for Computer Architects, Second Edition Tzvetan Metodi, Arvin I. Faruque, 2022-06-01 Quantum computers can in theory solve certain problems far faster than a classical computer running any known classical algorithm While existing technologies for building quantum computers are in their infancy it is not too early to consider their scalability and reliability in the context of the design of large scale quantum computers To architect such systems one must understand what it takes to design and model a balanced fault tolerant quantum computer architecture The goal of this lecture is to provide architectural abstractions for the design of a quantum computer and to explore the systems level challenges in achieving scalable fault tolerant quantum computation In this lecture we provide an engineering oriented introduction to quantum computation with an overview of the theory behind key quantum algorithms Next we look at architectural case studies based upon experimental data and future projections for quantum computation implemented using trapped ions While we focus here on architectures targeted for realization using trapped ions the techniques for quantum computer architecture design quantum fault tolerance and compilation described in this lecture are applicable to many other physical technologies that may be viable candidates for building a large scale quantum computing system We also discuss general issues involved with programming a quantum computer as well as a discussion of work on quantum architectures based on quantum teleportation Finally we consider some of the open issues remaining in the design of quantum computers

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Basic Elements for Quantum Computation Key Quantum Algorithms Building Reliable and Scalable Quantum Architectures
 Simulation of Quantum Computation Architectural Elements Case Study The Quantum Logic Array Architecture
 Programming the Quantum Architecture Using the QLA for Quantum Simulation The Transverse Ising Model Teleportation
 Based Quantum Architectures Concluding Remarks *Quantum Computer Systems* Yongshan Ding, Frederic T.
 Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer
 systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of
 this new paradigm of computing from a computer systems point of view without assuming any background in quantum
 mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental
 principles of the quantum theory and their implications for computing The second part is devoted to state of the art research
 in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware
 components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable
 progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and
 engineers can play to enable practical scale quantum computing **Multi-Core Cache Hierarchies** Rajeev
 Balasubramonian, Norman P. Jouppi, Naveen Muralimanohar, 2022-06-01 A key determinant of overall system performance
 and power dissipation is the cache hierarchy since access to off chip memory consumes many more cycles and energy than
 on chip accesses In addition multi core processors are expected to place ever higher bandwidth demands on the memory
 system All these issues make it important to avoid off chip memory access by improving the efficiency of the on chip cache
 Future multi core processors will have many large cache banks connected by a network and shared by many cores Hence
 many important problems must be solved cache resources must be allocated across many cores data must be placed in cache
 banks that are near the accessing core and the most important data must be identified for retention Finally difficulties in
 scaling existing technologies require adapting to and exploiting new technology constraints The book attempts a synthesis of
 recent cache research that has focused on innovations for multi core processors It is an excellent starting point for early
 stage graduate students researchers and practitioners who wish to understand the landscape of recent cache research The
 book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI
 engineers Table of Contents Basic Elements of Large Cache Design Organizing Data in CMP Last Level Caches Policies
 Impacting Cache Hit Rates Interconnection Networks within Large Caches Technology Concluding Remarks
Power-Efficient Computer Architectures Magnus Sjölander, Margaret Martonosi, Stefanos Kaxiras, 2022-05-31 As
 Moore's Law and Dennard scaling trends have slowed the challenges of building high performance computer architectures
 while maintaining acceptable power efficiency levels have heightened Over the past ten years architecture techniques for
 power efficiency have shifted from primarily focusing on module level efficiencies toward more holistic design styles based

on parallelism and heterogeneity This work highlights and synthesizes recent techniques and trends in power efficient computer architecture Table of Contents Introduction Voltage and Frequency Management Heterogeneity and Specialization Communication and Memory Systems Conclusions Bibliography Authors Biographies

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