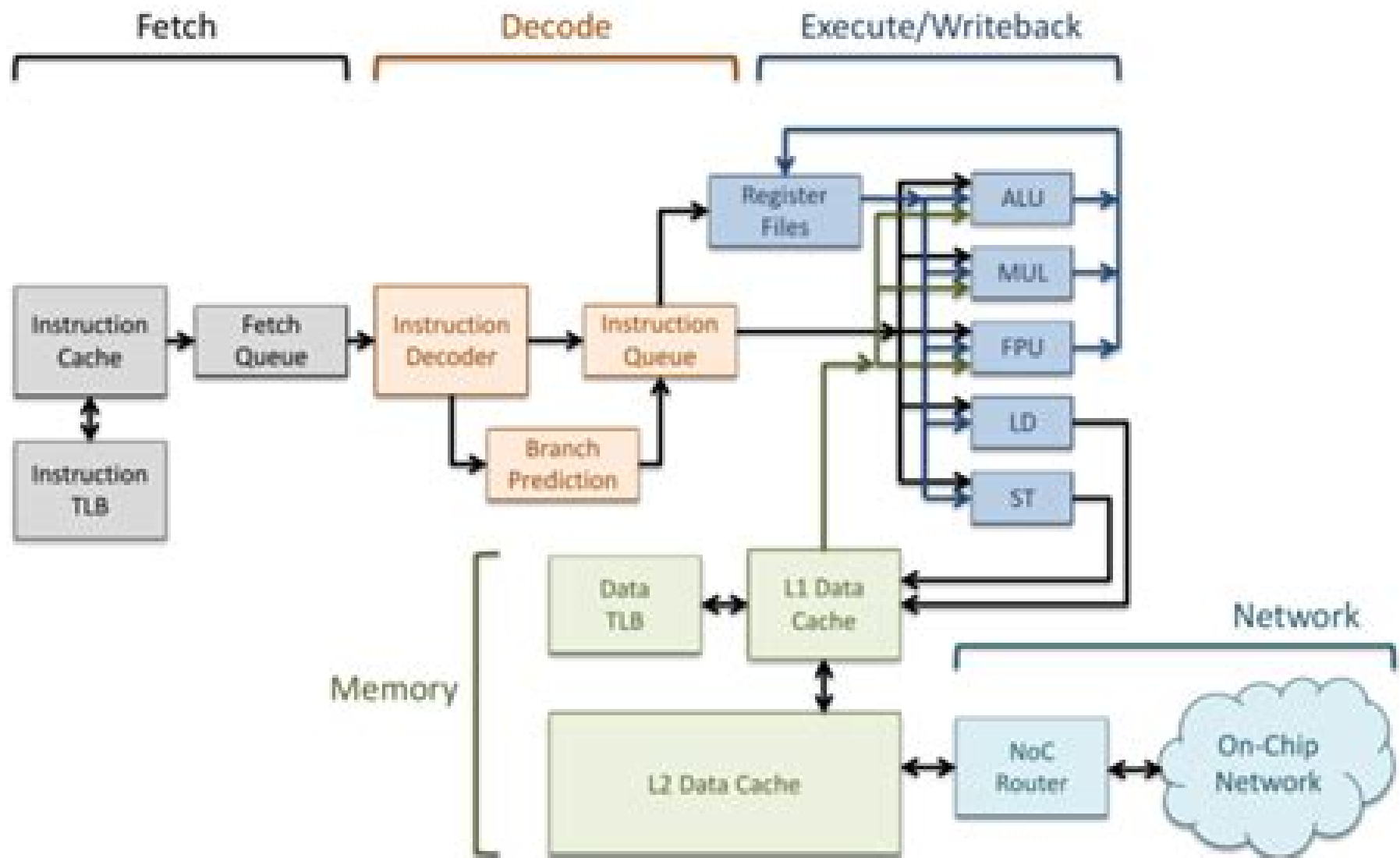


Processor Microarchitecture



Processor Microarchitecture Processor Microarchitecture

Daniel Kusswurm



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Microarchitecture of VLSI Computers P. Antognetti, F. Anceau, J. Vuillemin, 2012-12-06 Proceedings of the NATO Advanced Study Institute SOGESTA Urbino Italy July 9 20 1984

Modern X86 Assembly Language Programming Daniel Kusswurm, 2018-12-06 Gain the fundamentals of x86 64 bit assembly language programming and focus on the updated aspects of the x86 instruction set that are most relevant to application software development This book covers topics including x86 64 bit programming and Advanced Vector Extensions AVX programming The focus in this second edition is exclusively on 64 bit base programming architecture and AVX programming Modern X86 Assembly Language Programming s structure and sample code are designed to help you quickly understand x86 assembly language programming and the computational capabilities of the x86 platform After reading and using this book you ll be able to code performance enhancing functions and algorithms using x86 64 bit assembly language and the AVX AVX2 and AVX 512 instruction set extensions What You Will Learn Discover details of the x86 64 bit platform including its core architecture data types registers memory addressing modes and the basic instruction set Use the x86 64 bit instruction set to create performance enhancing functions that are callable from a high level language C Employ x86 64 bit assembly language to efficiently manipulate common data types and programming constructs including integers text strings arrays and structures Use the AVX instruction set to perform scalar floating point arithmetic Exploit the AVX AVX2 and AVX 512 instruction sets to significantly accelerate the performance of computationally intense algorithms in problem domains such as image processing computer graphics mathematics and statistics Apply various coding strategies and techniques to optimally exploit the x86 64 bit AVX AVX2 and AVX 512 instruction sets for maximum possible performance Who This Book Is For Software developers who want to learn how to write code using x86 64 bit assembly language It s also ideal for software developers who already have a basic understanding of x86 32 bit or 64 bit assembly language programming and are interested in learning how to exploit the SIMD capabilities of AVX AVX2 and AVX 512

Computer Architecture John L. Hennessy, David A. Patterson, 2006-11-03 The era of seemingly unlimited growth in processor performance is over single chip architectures can no longer overcome the performance limitations imposed by the power they consume and the heat they generate Today Intel and other semiconductor firms are abandoning the single fast processor model in favor of multi core microprocessors chips that combine two or more processors in a single package In the fourth edition of Computer Architecture the authors focus on this historic shift increasing their coverage of multiprocessors and exploring the most effective ways of achieving parallelism as the key to unlocking the power of multiple processor architectures Additionally the new edition has expanded and updated

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Temam,2010-09-15 Simulation of computer architectures has made rapid progress recently The primary application areas are hardware software performance estimation and optimization as well as functional and timing verification Recent innovative technologies such as retargetable simulator generation dynamic binary translation or sampling simulation have enabled widespread use of processor and system on chip SoC simulation tools in the semiconductor and embedded system industries Simultaneously processor and SoC simulation is still a very active research area e g what amounts to higher simulation speed flexibility and accuracy speed trade offs This book presents and discusses the principle technologies and state of the art in high level hardware architecture simulation both at the processor and the system on chip level

Processor Architecture Jurij Silc,Borut Robic,Theo Ungerer,2012-12-06 Today s microprocessors are the powerful descendants of the von Neumann 1 computer dating back to a memo of Burks Goldstine and von Neumann of 1946 The so called von Neumann architecture is characterized by a sequential control flow resulting in a sequential instruction stream A program counter addresses the next instruction if the preceding instruction is not a control instruction such as e g jump branch subprogram call or return An instruction is coded in an instruction format of fixed or variable length where the opcode is followed by one or more operands that can be data addresses of data or the address of an instruction in the case of a control instruction The opcode defines the types of operands Code and data are stored in a common storage that is linear addressed in units of memory words bytes words etc The overwhelming design criterion of the von Neumann computer was the minimization of hardware and especially of storage The most simple implementation of a von Neumann computer is characterized by a microarchitecture that defines a closely coupled control and arithmetic logic unit ALU a storage unit and an I O unit all connected by a single connection unit The instruction fetch by the control unit alternates with operand fetches and result stores for the ALU

System-on-Chip Test Architectures Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test

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